I CLAIM:

1. A substrate for a package of high frequency semiconductor devices, comprising:

a planar insulating substrate having a plurality of parallel, planar metal layers embedded in said insulator;

at least one pair of parallel, metal-filled vias traversing said substrate, said vias having a diameter and a distance from each other of at least said diameter, said vias connecting metal ports on said substrate; and

said metal in each via having a sheet-like extension in each of selected planes of said metal layers.

2. The substrate according to Claim 1 wherein said sheet-like metal extensions are configured so that each extension enhances the electrical via-to-via capacitance, and the sum of said increased capacitances reduces the reflection of a high-frequency signal arriving at said via ports to less than 10 %.

3. The substrate according to Claim 1, wherein said metal extensions are shaped approximately as rings, which surround each via in the plane of each metal layer, said extensions attached to the via metal.

4. The substrate according to Claim 3 wherein said rings have straight perimeter portions where they are in close proximity to respective extensions attached to neighboring vias.

5. The substrate according to Claim 4 wherein said proximity of said neighboring straight perimeter portions is at least 50 % of the layer thickness of said metal extensions.

6. The substrate according to Claim 1, wherein said metal extensions are shaped as flat forks arranged so that, in one plane of said metal layers, the fork of the first via of said pair is oriented towards, and partially surrounds, the second via of said pair, while in the next plane of said metal layers, the fork of said second via is oriented towards, and partially surrounds, said first via of said pair.

7. The substrate according to Claim 1 wherein said vias have a diameter from about 0.1 to 0.3 mm, and a distance from each other from about 0.1 to 0.3 mm.

8. A high frequency semiconductor device comprising:

a semiconductor chip having at least one pair of bond pads;

a planar insulating substrate having a plurality of parallel, planar metal layers embedded in said insulator and input/output ports on the first and second substrate surface;

said substrate having at least one pair of parallel, metal-filled vias traversing said substrate, said vias having a diameter and a distance from each other of at least said diameter, said vias connecting said metal ports on said first and second surface, said metal in each via having a sheet-like extension in each of selected planes of said metal layers;

said chip assembled on said first substrate surface so that said at least one pair of chip bond pads is connected to one pair of said substrate ports on said first substrate surface, respectively; and

interconnection elements attached to said ports on

said second substrate surface for connection to external parts.

9. The device according to Claim 8 wherein said sheet-like metal extensions are configured so that each extension enhances the electrical via-to-via capacitance, and the sum of said increased capacitances reduces the reflection of a high-frequency signal arriving at said via ports on said first or second substrate surface to less than 10 %.

10. The device according to Claim 8 wherein said connections between said pair of chip bond pads and said substrate ports on said first substrate surface are metal bumps.

11. The device according to Claim 8 wherein said connections between said pair of chip bond pads and said substrate ports on said first substrate surface are bonding wires.

12. The device according to Claim 8 wherein said interconnection elements are metal reflow bumps.

13. A method of fabricating a laminated substrate having a plurality of parallel, planar metal layers separated by insulating layers for use in high frequency semiconductor packages, comprising the steps of:

etching electrical traces into the metal layer of the first metal-on-insulator pair, while concurrently etching a plurality of metal geometries separate from said traces;

repeating said etching step of respective electrical traces and geometries for each successive metal-on-insulator pair, after each pair has been added in planar position onto the previous pair, thus creating step by step a stack of vertically

aligned metal geometries;

opening a via in the location of each stack of said plurality; and

filling said vias with metal so that electrical contact between said via metal and each respective metal geometry of each stack is established and said geometries are transformed into extensions of the respective via metal.

14. The method according to Claim 13 wherein said vias have a diameter and a distance from each other of at least said diameter.